

UW-MEMS DESIGN HANDBOOK

VERSION 3.0



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CHAPTER 1: GOLD BASED SURFACE MICROMACHINING PROCESS

INTRODUCTION

The UW-MEMS Process is a research oriented cost effective, proof of concept, multi-user MEMS fabrication process for industries, universities and government agencies offered at the University of Waterloo, Waterloo, Ontario, Canada. The process is a gold-based surface micromachining process derived from work carried out by the University of Waterloo over the past 6 years. It has been used successfully to build several MEMS devices [1] - [8].

The following is a general process description and user guide for the UW-MEMS process which is optimized for general RF applications. Nevertheless, the process is also applicable to many other MEMS devices. MEMS designers from all engineering disciplines are encouraged to submit their designs. These guidelines are written for users with a minimum of processing experience. Design rules are provided in Chapter 2. A detailed example is given in Chapter 3 illustrating the typical layouts designers need to submit to the UW-MEMS process

PROCESS OVERVIEW

The UW-MEMS process is a seven mask process developed and optimized at the University of Waterloo, Center for Integrated RF Engineering (CIRFE). The process starts with a 0.025" thick Alumina substrate polished on both sides. The relative permittivity of the substrate is 9.8 with loss tangent of 0.0001 at 1MHz. The masks that are used for the process are E-beam-write chrome masks.

MASK #1 CHROMIUM

After the RCA cleaning of the wafer, the first layer of Cr is deposited and patterned using the lift-off technique.

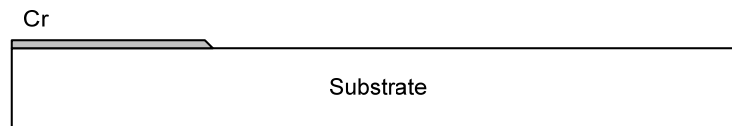


Figure 1.1: Mask #1 patterning

MASK #2 DIELECTRIC 1

A 0.5 μm of PECVD Silicon Oxide is deposited and patterned. RIE is employed to pattern the oxide and remove the patterning photo resist.

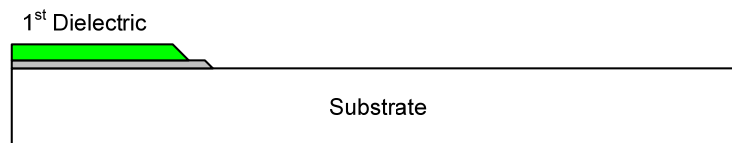


Figure 1.2: Mask #2 Patterning

MASK #3 GOLD 1

An evaporated 400\AA chromium / 100nm gold bilayer is deposited as a seed layer. A PR mould is formed in the third lithographic step and $1\mu\text{m}$ gold is electroplated inside the mould. The mould and seed layers will be removed afterwards. The chromium is applied as an adhesion layer for the gold.

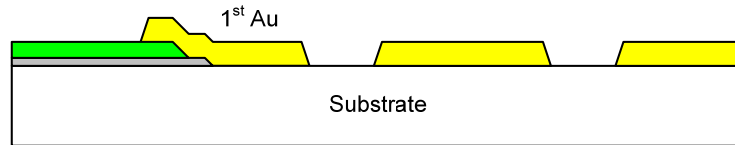


Figure 1.3: Mask #3 Patterning

MASK #4 DIELECTRIC 2

A 300\AA of chromium (Cr) film is sputtered followed by the deposition of $0.7\mu\text{m}$ silicon oxide using plasma enhanced chemical vapour deposition (PECVD) at 250°C . The dielectric and Cr layers are dry and Wet etched, respectively. The Cr layer serves as an adhesion layer for the silicon oxide to the gold.

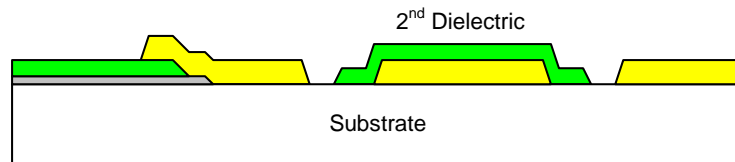


Figure 1.4: Mask #4 Patterning

MASK #5 ANCHOR

Spin coated Polyimide is used as the sacrificial layer for this process. Initially, it is coated to a thickness of $2.5\mu\text{m}$. Next, it is patterned by Mask#5 (anchor mask) in an RIE step to etch the PI and fully clear the anchor holes.

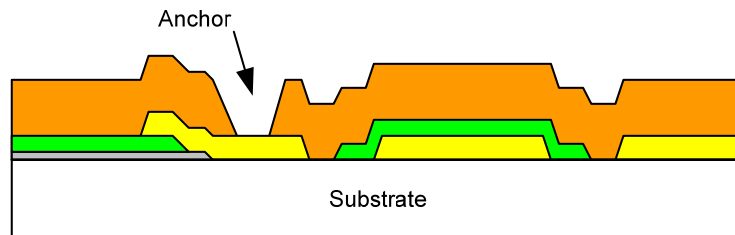


Figure 1.5: Mask #5 Patterning

MASKS #6 DIMPLE

Photo resist mask is used to pattern the dimples in an RIE etching step. The depth of the etching is controlled to be 1µm.

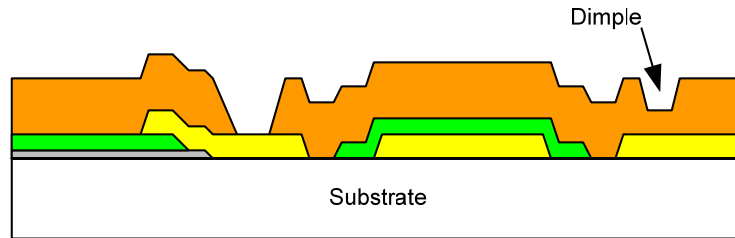


Figure 1.6: Masks #6 Patterning

MASK #7 GOLD 2

The top gold layer consists of a sputtered gold seed layer and an electroplated gold. The total thickness of this layer is 1.25µm, and it is used as the structural layer for the devices. Moulding Method is used to define this layer.

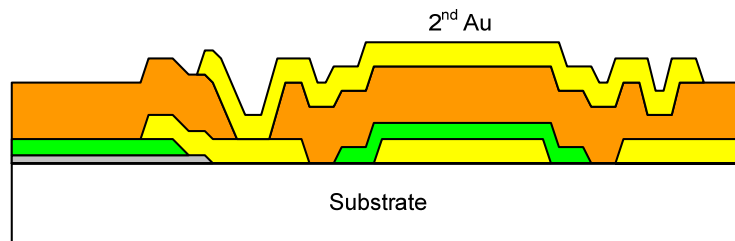


Figure 1.7: Masks 7 Patterning

RELEASE PROCESS

The wafers are diced into individual dies and the sacrificial layer is removed in an oxygen plasma dry etch process. At this stage, the fabrication is complete and samples are packaged for shipping to the customers.

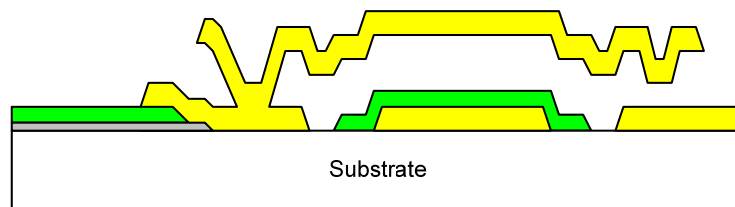


Figure 1.8: Released Device

CHAPTER 2: UW-MEMS PROCESS DESIGN GUIDELINES

INTRODUCTION

These design guidelines and rules were determined during the process development stage and several fabrication runs carried out at the University of Waterloo's CIRFE facility. These rules identify the physical limitations of individual process steps. These guidelines and rules are extremely important and needed to be considered at the design stage. If the guidelines are not respected, the device will not meet the specifications and will most likely fail or malfunction.

In general there are two types of rules. The first type of rules specifies the minimum feature and gap sizes. Minimum feature size refers to the minimum width of a trace that will be feasible using the current process. In other words, if this rule is violated there is no

guarantee that the feature will be produced on the wafer. In the same way, the minimum gap specifies the shortest separation distance between two adjacent features. Failure to follow this rule results in a merged feature consisting of the later patterns. The second type of rules specifies the crossovers and inter-level spacing. This relates to the alignment of the layers and will be shortly detailed. Both rule types are considered mandatory and should be followed by the designer.

DESIGN RULES: GENERAL OUTLINES

Design rules for the UW-MEMS process are explained in the following tables and illustrated in schematic format. Table 1 outlines the materials, thicknesses and mask levels for each layer. A brief description of each layer with comments is also included.

Table 1: Layer Names, Thickness and Mask Level

Material	Thickness μm	Mask Level	Layer Description	Comments
Cr Chromium	0.04	Mask #1	Resistive Voltage Biasing	Resistive Layer
D1 Silicon Oxide	0.5	Masks #2 & #3	Dielectric	Dielectric to cover Cr
G1 Gold 1	1	Mask #4	Conductive Layer	400Å Cr + 1μm Au
D2 Silicon Oxide	0.7	Mask #5	Dielectric	300Å Cr + 0.7μm SiO ₂
Sacrificial Layer	2.5	Masks #6 & #7	Sacrificial Layer	2.5μm Anchor and 1μm Dimple Openings
G2 Gold 2	1.25	Mask #8 & #9	Top Conductive Layer	0.1μm Sputtered Au + 1.15μm Electroplated Au

Table 2 outlines the mask levels that are used during the process. Please note that for the “Light” field you draw the parts you want to be remained on the wafer. For example, for Mask #1 (Cr layer patterning) you draw the traces such as bias lines. For the “Dark” field you draw the parts you want to be removed from the corresponding layer such as holes. For example, to create an anchor you draw a hole. For Mask#7 you draw the squares where you want to create dimples. Please pay special attention to this concept. Failure to do so will result in a reverse polarity devices. For Mask #3 and Mask#9 (Openings in D1 and Release Holes in Gold 2), the designer should draw the location of openings and release holes, respectively. These layers will be subtracted from the D1 and G2 layers by the University of Waterloo personnel prior to making the masks #2 and #8.

Table 2: Lithography Mask Levels

Mask levels	Field Type	Comments
Mask #1	Light	Patterning Cr
Mask #2	Light	Patterning D1
Mask #3	Dark	Additional layer for openings on the D1 layer
Mask #4	Light	Patterning G1
Mask #5	Light	Patterning D2
Mask #6	Dark	Opening Anchors for G1 and G2 Connection
Mask #7	Dark	Dimples for G2 For contacts of the switches as well as preventing the stiction of large plates
Mask #8	Light	Patterning G2
Mask #9	Dark	Additional layer for release holes of the G2 layer.

Table 3 presents the mask levels with their respective GDS numbers. GDS is the format that UW MEMS will accept. Please use the GDS numbers that are specified in the table for each layer to avoid any confusion. Masks 3 and 9 are only to create the openings in the D1 layer and the release holes on G2 layer, respectively and not for processing purposes.

Table 3: UW MEMS Process GDS Number, Minimum Features and Gaps

Mask Level	Layer Name	GDS #
Mask 1	Cr	101
Mask 2	D1	102
Mask 3	D1HOLE	110
Mask 4	G1	103
Mask 5	D2	104
Mask 6	Anchor	105
Mask 7	Dimple	106
Mask 8	G2	107
Mask 9	G2R	109

Please note that the dimples are meant for small features. Nominal surface area is 10 μ m by 10 μ m. However, they can be used for long lines, but it is recommended that the width of the lines be 10 μ m.

DESIGN RULES: OVERLAPS & ENCLOSURES

Generally, for any design, the following guidelines should be considered:

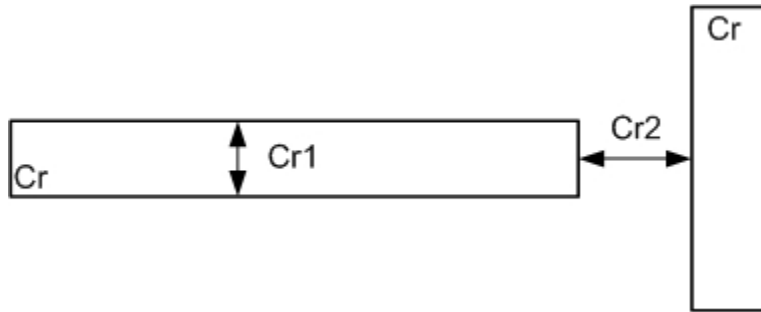
- For overlaps and enclosure of the layers, up to 10 μ m of misalignment between the layers is possible. This is due to the limitations of our lithography system. This is an advisory rule.
- Cr lines are designated for the DC bias lines with no current flow. This layer is very thin, and it is not intended for power transfer.

The following outlines the specific rules to which close attention must be paid during the design stage. Please note that the minimum feature size and minimum spacing are limits to which the designers should strictly adhere. Ideally, adding a 10 μ m additional safety margin to these numbers may increase the chance of success. You can have round,

orthogonal or any arbitrary shape in your layout.

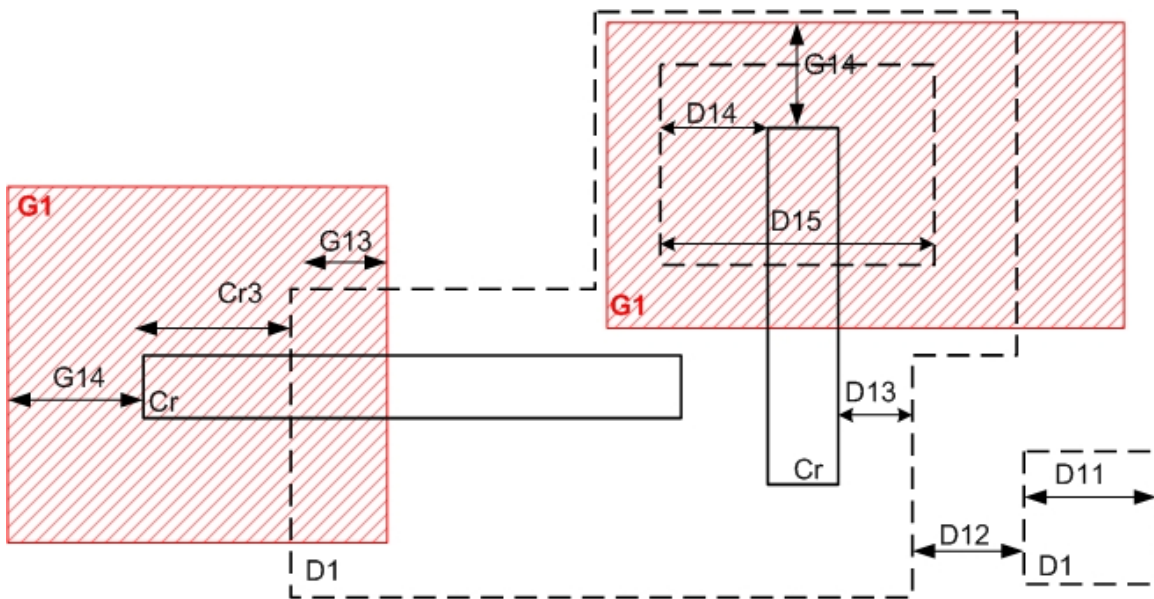
The release holes must be 10 μ m x 10 μ m squares with edge to edge distances not exceeding 25 μ m. Please do not use this layer to define geometries. The features are embedded to provide access to underneath the structural layer during the release purposes.

1- Cr –DC bias lines:



Description	Rule Label	Value(μm)
Minimum width/length	Cr1	≥ 10
Minimum distance	Cr2	≥ 10

2- Dielectric1 (D1) stacked with Cr and Gold 1 (G1)

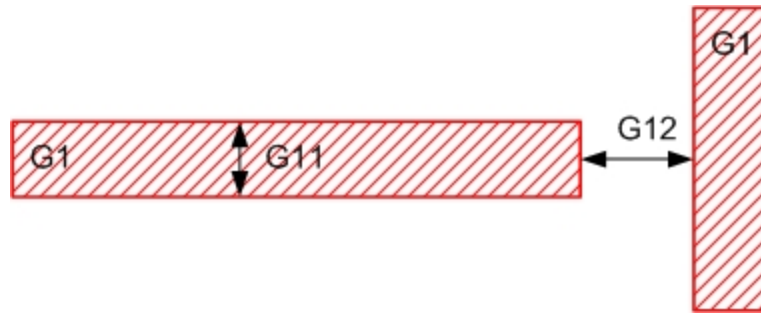


Description	Rule Label	Value(μm)
Minimum extension of Cr connecting pad from D1	Cr3	≥ 20
Minimum width, length of D1	D11	≥ 15
Minimum D1 to D1 distance	D12	≥ 15
D1 Overlap over Cr-bias lines	D13	≥ 5
Minimum extension of D1HOLE from Cr	D14	≥ 10
Minimum width, length of D1HOLE	D15	≥ 35

G1 overlap with Cr/D1	G13	≥ 15
G1 overlap with Cr connecting pad	G14	≥ 10

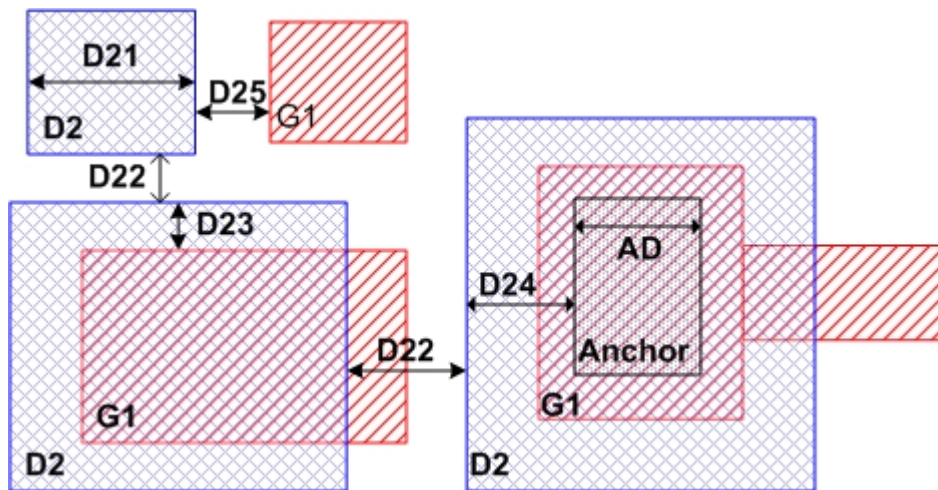
Note: Cr MUST be always covered with D1, G1, or both.

3- Gold 1 (G1)



Description	Rule Label	Value(μm)
Minimum width, length	G11	≥ 10
Minimum distance	G12	≥ 10

4. Dielectric 2 and Cr as adhesion layer (D2)

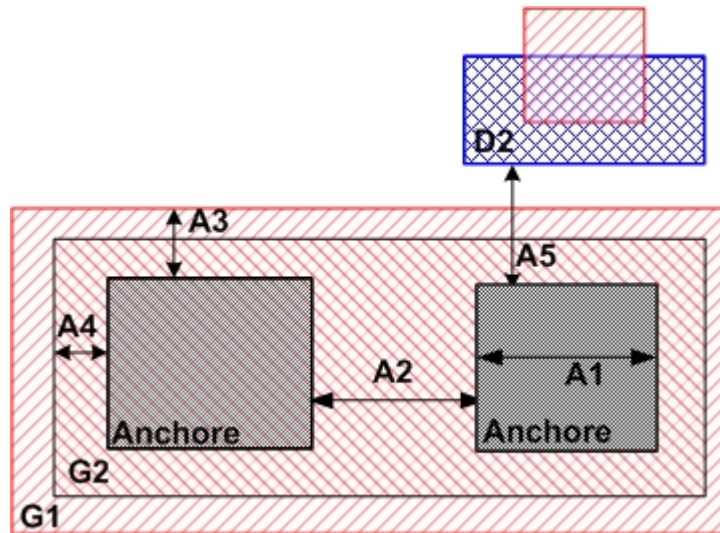


Description	Rule Label	Value(μm)
Minimum width, length for D2	D21	≥ 15
Minimum Distance for D2 (D2 covering two trances MUST be separated)	D22	≥ 15
D2 overlap with G1	D23	≥ 10

D2 overlap with Anchor	D24	≥ 15
D2 distance from G1	D25	≥ 15
Maximum anchor size over D2 *	AD	≤ 200

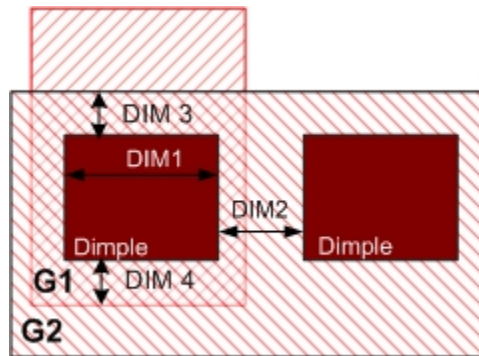
* Anchor on top of D2 can not be used as mechanical support but can be used for metal-insulator-metal (MIM) capacitor.

5. Anchor



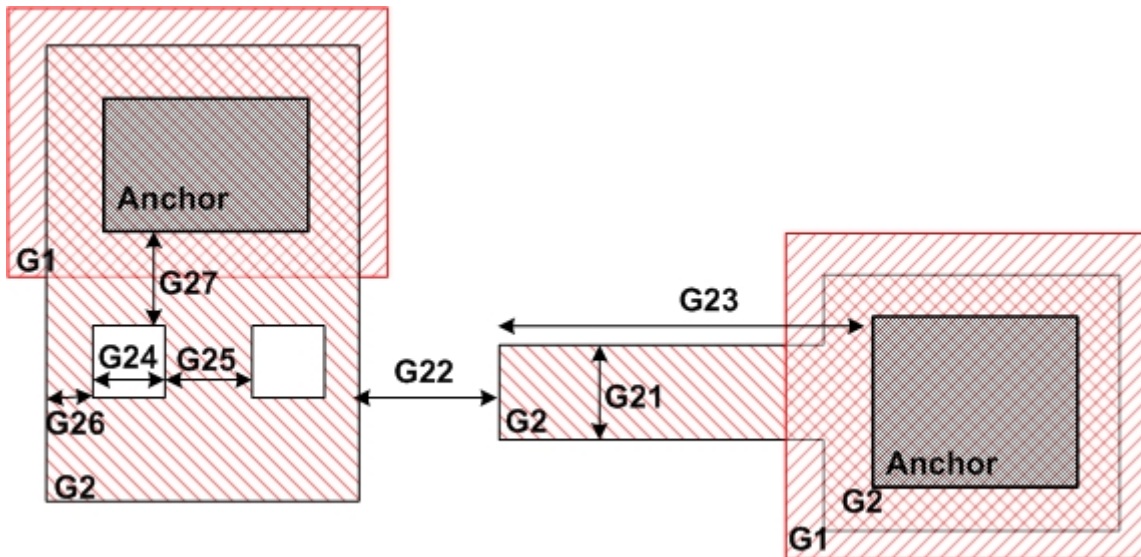
Description	Rule Label	Value(μm)
Minimum width, length	A1	≥ 10
Minimum distance	A2	≥ 10
Minimum G1 overlap with Anchor (Anchor MUST be covered with G1)	A3	≥ 10
Minimum G2 overlap with Anchor (Anchor MUST be covered with G2)	A4	≥ 5
Minimum distance of D2 with Anchor	A5	≥ 10

6. Dimple



Description	Rule Label	Value(μm)
Minimum width, length	DIM 1	≥ 10
Minimum distance	DIM 2	≥ 10
Minimum G2 overlap with Dimple	DIM 3	≥ 5
Minimum G1 overlap with dimple	DIM4	≥ 5

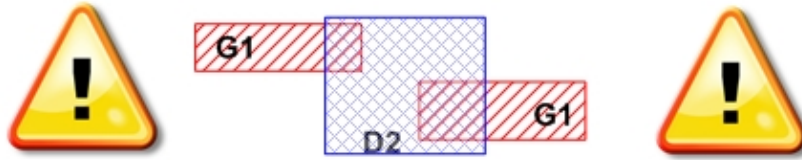
7. Gold 2 (G2)



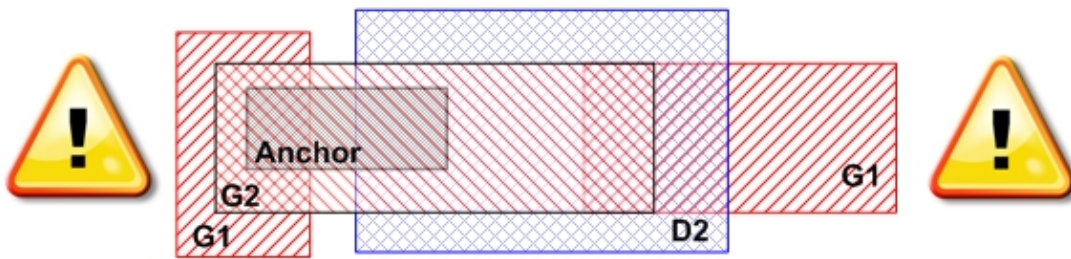
Description	Rule Label	Value(μm)
Minimum width, length	G21	≥ 10
Minimum distance	G22	≥ 10
Maximum ratio of G23/G21 when G2 is not anchored	G23/G21	≤ 30
Maximum non anchored G2 length	G23	≤ 1200

Release Hole minimum size	G24	≥ 10
Maximum distance between the release holes	G25	$25 \geq$
Minimum distance of the release hole and the edge	G26	≥ 10
Maximum, Minimum release hole distance from anchor	G27	$\geq 10 , \leq 30$

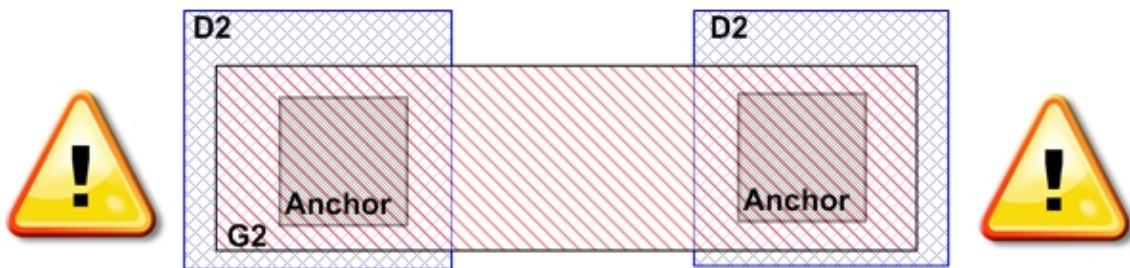
Caution



D2 covering two G1 traces may result in short circuit between the two G1 traces!



All G1 and G2 traces may be shorted through D2!



G2 does not have proper mechanical support and may be damaged during fabrication!

MATERIAL PROPERTIES

Table 4 reports some of the mechanical and electrical properties of the UW-MEMS process. The data is based on the measurements performed on earlier UW-MEMS processes and agree well with the nominal known values in the literature. Designers can use the existing values in the literature for the other material properties.

Table 4: Material properties of UW MEMS process

Material Name	Residual Stress (MPa)	Conductivity (Siemens/m)	Sheet Resistance Ω/sq	Relative Permittivity
Cr	1200	-----	20 *	-----
G1	190 +/- 30% Tensile	3.6×10^7	-----	-----
SiO2	-----	-----	-----	4
G2	190 +/- 30% Tensile	3.6×10^7	-----	-----

* A higher resistivity (500 Ω /sq) will be optionally available

CHAPTER 3: AN EXAMPLE

LAYOUT GENERATION

This chapter presents a simple example of a MEMS relay to illustrate the layout generation process step-by-step for designers. Experienced designers typically use tools such as L-EDIT and Cadence to generate the layouts for the various masks. However, any tool that can generate layouts in GDSII formats can be used to submit designs to the UW-MEMS process. This example is given to provide beginners in the field with layout illustrations to help them understand the design guidelines given in Chapter 2. Therefore, Chapter 2 must be read first.

Consider the MEMS relay shown in Figure 3.1. It consists of a cantilever anchored to an input signal line. The cantilever can be pulled down using electrostatic actuation so that its tip makes contact with the output signal line and hence closes the relay. The electrostatic actuation is provided using an actuation pad covered by oxide (as an insulator). The two dc bias pads are connected to the actuation pad and the input signal line using high resistivity Chromium traces. A dimple is added to the cantilever tip to ensure contact with the output signal line. It should be noted that such a simple relay requires extensive analysis and characterization for proper selection of dimensions to achieve a working prototype. Below is a description of the six masks used for production of a MEMS relay.

- Figure 3.2a shows the layout of Mask #1 (Cr Layer). This mask shows the two high resistivity traces that connect the dc bias pads to the actuation pad and the input signal line. The field type of this mask is "light". Note that the Cr traces must be made at least 20 μm longer on each side in order to overlap the gold (see Design Rules: Overlaps & Enclosures).
- Figure 3.2b shows the layout of Mask #2, 3 (Oxide Layer). This mask shows the insulation layer that covers the bias lines. The field type of this mask is "light".
- Figure 3.2c shows the layout of Mask #4 (G1 Layer). This mask shows the input/output signal lines, actuation electrode and the two bias pads. Note that the field type of this mask is "light" (See Table 2).
- Figure 3.2d shows the layout of Mask #5 (Oxide Layer). This mask shows the insulation layer that covers the actuation electrode. The field type of this mask is "light".
- Figure 3.2e Shows the layout of Mask #6 (Anchor). This mask defines the anchor location for connection of G2 and G1. The field type of this mask is "dark" (the designer needs to draw the parts that will be removed from the sacrificial layer).
- Figure 3.2f shows the layout of Mask #7 (Dimple). This mask illustrates the dimples which are connected to the tip of the cantilever. The field type of this mask is "dark".
- Figure 3.2g shows the layout of Mask #8 (G2 Layer). This mask shows the cantilever. The field type of this mask is "light". Note that the cantilever length needs to be extended at the anchor location in order to make sure that G1 and

G2 enclose the anchor (see Design Rules: Overlaps & Enclosures).

- Figure 3.2h shows the layout of Mask #9 (Release holes). This layer will be subtracted from G2 layer mask by the University of Waterloo personnel to generate the final Mask.

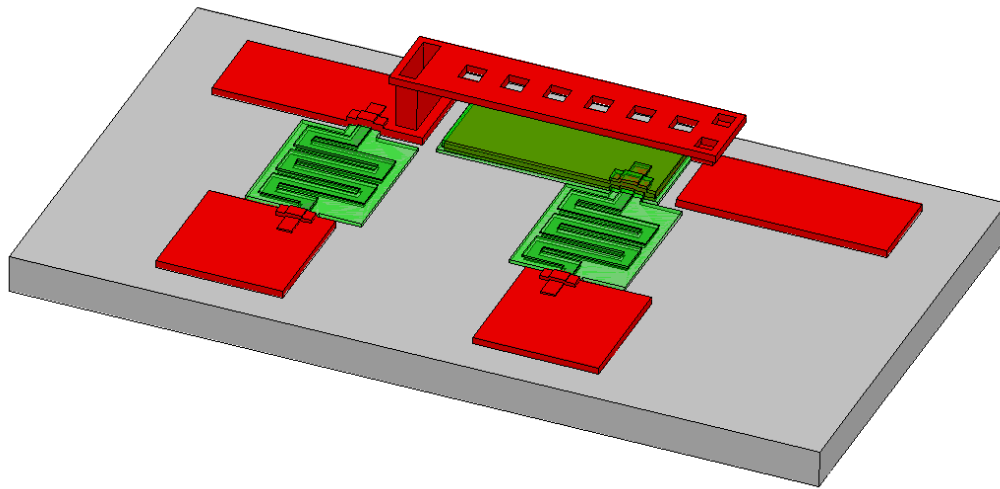


Figure 3.1: A MEMS Relay

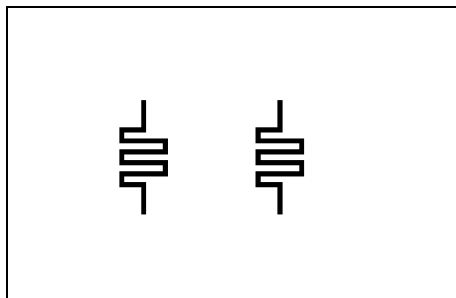


Figure 3.2a: Mask #1

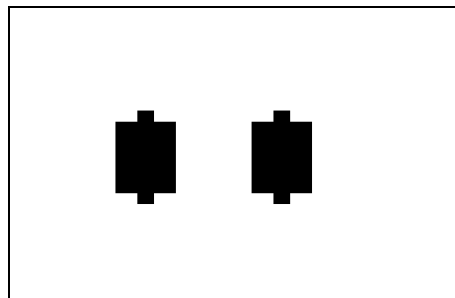


Figure 3.2b: Mask #2,3

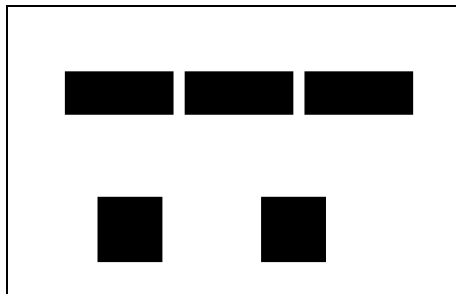


Figure 3.2c: Mask #4

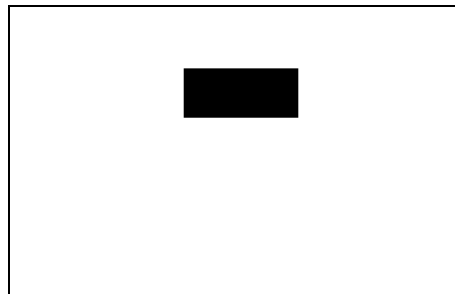


Figure 3.2d: Mask #5

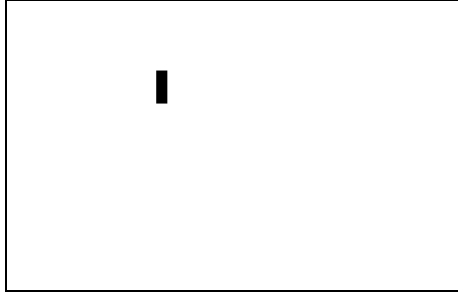


Figure 3.2e: Mask #6

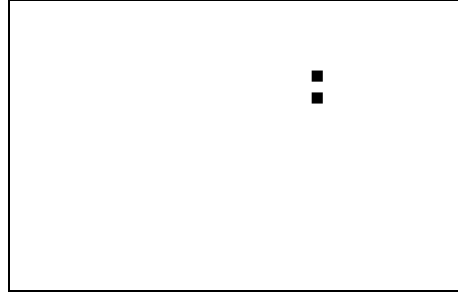


Figure 3.2f: Mask #7

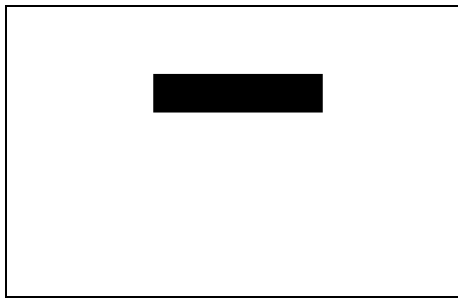


Figure 3.2g: Mask #8

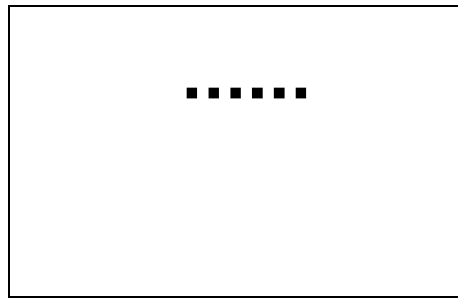


Figure 3.2h: Mask #9

CHAPTER 4: DESIGN SUBMISSION

UW-MEMS SUBMISSION FILE FORMAT

Designs should be submitted in GDSII format. Tanner L-Edit is the recommended layout software. However, most of the other layout software tools can export to GDS format including Coventor-Ware. A template for this process can be found on our website. The layers should match the numbers posted in Table 3 of this handbook.

Please visit our website for more information:

www.cirfe.uwaterloo.ca

CUSTOM UW-MEMS PROCESS

CUSTOM UW-MEMS PROCESSES

The CIRFE facility has capability to provide a modified version of the UW-MEMS process on a case by case basis. Designers will be able to select thickness of materials, type of structural and sacrificial layers and number of layers. The CIRFE facility also offers a variety of thin film metal and dielectric deposition services.

For inquiry about the CUSTOM UW-MEMS Processes, please e-mail:
uwmems@mems.uwaterloo.ca

CONTACT INFORMATION

For questions or general inquiry about the UW-MEMS process, please send your e-mails to:

uwmems@mems.uwaterloo.ca

Updates to this design handbook and further details about the CIRFE facility can be found on our website at:

www.cirfe.uwaterloo.ca

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